Complementary 2-D MESFET for Low Power Electronics

Interim Report # 2

Air Force SBIR Phase I
Contract Number: F33615-95-C-1679

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Phase I Interim Report #2

As detailed in the Phase I proposal, the project has four major tasks. These are 1) assessment of the p-channel 2-D MESFET device fabrication, 2) development of a p-channel 2-D MESFET model and implementation of the model into AIM-SPICE, 3) circuit simulations of complementary 2-D MESFET circuits using AIM-SPICE and comparison with conventional circuits, and, 4) analysis of manufacturability and technology insertion issues. This report summarizes progress in each task area during the period 17 MAY 95 -3 JUN 95.

Task 1: Assessment of p-Channel Device Fabrication

The assessment of the p-channel 2-D MESFET device fabrication is underway. Heterostructure modeling of a prospective AlGaAs/InGaAs/GaAs structure has been performed to predict the valence band and carrier distributions prior to procurement of the wafer. The structure will be ordered within the month. Once the wafer is delivered, the p-channel device fabrication will commence.

Task 2: Development of p-Channel 2-D MESFET Model

The initial development of a p-channel 2-D MESFET model is also underway. Presently, we are using the n-channel model with realistic values for the hole mobility, saturation velocity and Schottky barrier height to predict the current-voltage characteristics of p-channel 2-D MESFETs. These simulations indicate that hole sheet densities comparable to those used in the n-channel device will be appropriate for the p-channel device, and that similar channel geometries (i.e. channel widths of order 0.5 - 1.0 micron) are also appropriate. Thus, we will use our existing mask set and will complete the heterostructure design and procure the wafer for fabrication.

Task 3: Complementary 2-D MESFET Circuit Simulations

Circuit simulations of complementary 2-D MESFET circuits will take place later in the Phase I project.

Task 4: Manufacturability and Technology Insertion Issues

A comprehensive technology analysis of complementary 2-D MESFET circuits will be performed throughout the duration of the Phase I project. It will serve to summarize the main advantages of a complementary 2-D MESFET over existing technologies and to address any potential barriers to insertion of the complementary 2-D MESFET technology into the large scale IC manufacturing environment.

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